

# The design of a dynamic slope compensation circuit for boost DC-DC converter

**Zhao Han, Yuan Rao, Wentao Chen, Junkai Huang\***

*School of Information Science and Technology, Jinan University, Guangzhou, Guangdong Province, 510632, China*

*Received 6 April 2014, www.tsi.lv*

---

## Abstract

This paper proposes a structure of peak current mode Boost DC-DC converter with slope compensation circuit, and designs a dynamic slope compensation circuit applied to this converter. With the utilization of the voltage controlled resistance characteristics of MOS transistor and the introduction of a clamp circuit consist of cascade current mirror, a dynamic slope compensation circuit is realized. The circuit is simulated on Cadence Spectre using SMIC 0.18 $\mu$ m CMOS technology. Results show that it can provide proper slope compensation following the variation of input and output. The load capacity of DC-DC converter reaches 550mA and the transient response lows to 10  $\mu$ s. By eliminating the problem of instability caused by the peak current mode switching power supply of double loop control, the design improves the stability of switching power supply.

*Keywords:* boost DC-DC, slope compensation, current mirror, voltage controlled resistor

---

## 1 Introduction

With the rapid development of electronic devices, the requirements of the power supply with higher storage capacity and stability are growing rapidly. Though battery technologies have been developing fast, they still cannot meet these requirements. So more and more attentions have been draw to DC-DC switching power supply [1-3], which has high conversion efficiency and stability. However, in the peak current mode, the deviation between the peak inductive current and the average output current lowers the precision. Especially, there are several drawbacks such as sub-harmonic oscillation, open-loop instability and worse loop response when the duty cycle is over 50%. Therefore, the slope compensation circuit [4, 5] used to improve system performance has practical value. The fixed slope compensation and the piecewise linear slope compensation have been proposed in [6] and [7]. Nevertheless, these two slope compensation methods cannot adjust the slope compensation current dynamically with the changes in the duty cycle, and may cause excessive compensation or under compensation, which may lead to lower the transient response and load capability of the switching power supply.

Based on DC-DC converter, a low power, MOS tube consisted dynamic slope compensation circuit is proposed, which can automatically adjust the slope compensation current following the variation of input and output voltage, and the simulation of it is also conducted.

## 2 Peak Current Mode boost DC-DC converter

Based on the technical requirements of the Boost DC-DC converter [4], the proposed structure of peak current mode Boost DC-DC converter with slope compensation circuit is shown in Figure 1. Synchronous rectification with dead time is used in this structure to prevent the main power tubes and freewheeling tubes from conducting simultaneously. Moreover, the structure is controlled by two feedback loops. One is voltage feedback loop composed by the error amplifier which receives the output voltage sampling signal, and the other is current feedback loop composed by the peak current comparator which receives current sampling signal and slope compensation signal.

In Figure 1, error amplifier amplify the difference between the output voltage sampling signal  $V_{FB}$  and the reference voltage  $V_{REF}$ , and input the resulting voltage signal  $V_E$  to the peak current comparator. The inductive current signal  $V_S$  extracted by current sampling circuit and the slope compensation signal generated by slope compensation circuit are superimposed, and the result is inputted to the peak current comparator. The output control signals adjust conduction time of the power MOSFET to realize stability. So, the performance of slope compensation circuit plays a decisive role in realizing stability of the whole system. It can reduce or even eliminate the open-loop instability and other negative phenomena caused by inductive current disturbance.

---

\* *Corresponding author* e-mail: hjkeed@163.com

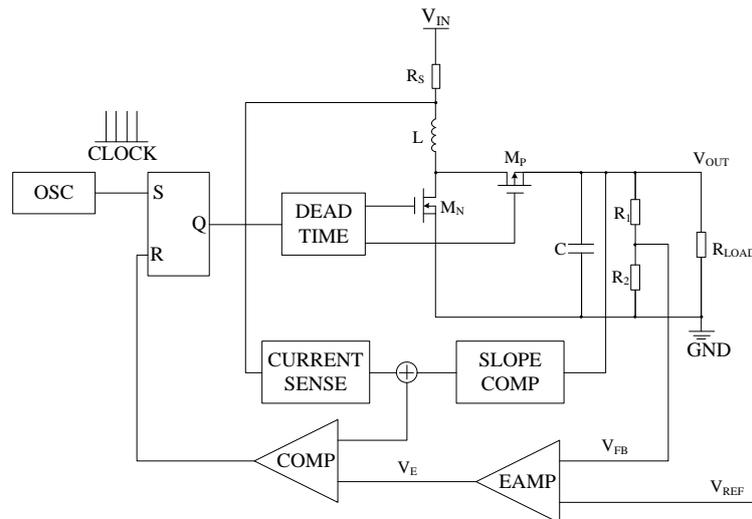


FIGURE 1 Structure of peak current mode Boost DC-DC converter

**3 Dynamic Slope Compensation Method and Design**

**3.1 THE BASIC PRINCIPLE OF SLOPE COMPENSATION**

Figure 2 shows the open-loop instabilities phenomena [2, 5] in the Boost DC-DC converter when duty cycle  $D$  is over 50%. Where  $V_E$  is the error amplifying signal of the voltage feedback loop,  $m_1$  and  $m_2$  represent the ascending slope and descending slope respectively, and  $\Delta I_0$  is the initial disturbance current.

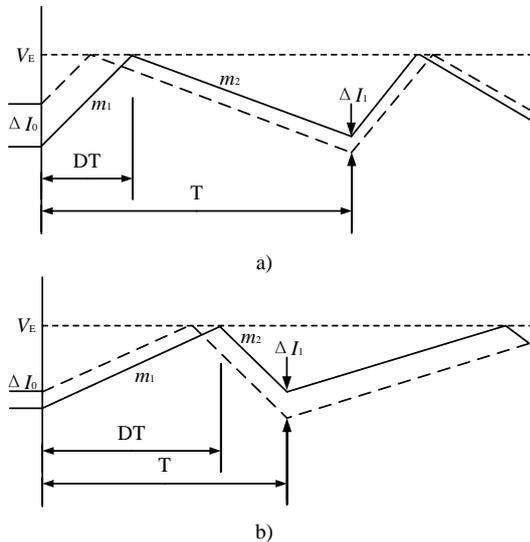


FIGURE 2 The instabilities of Boost DC-DC converter without slope compensation: a)  $D < 50\%$ , b)  $D > 50\%$

In Figure 2, the solid lines stand for the inductive current waveform when the circuit is stable, while the dashed lines stand for the same waveform when the circuit is disturbed. As we can see, when  $D < 50\%$ , the ratio  $m_2/m_1 < 1$ , the disturbance current is lowering, the system is stable. While  $D > 50\%$ , the ratio  $m_2/m_1 > 1$ , the disturbance current is rising, the open-loop is unstable.

Figure 3 presents the introduction of slope compensation when  $D > 50\%$ . To eliminate the open-loop

instability, the slope  $m$  of the introduced signal should satisfy the equation below:

$$\left| \frac{m_2 - m_1}{m_1 + m} \right| < 1 \tag{1}$$

In the Continue Conduction Mode (CCM) mode, the relationship between the slope  $m$  of the slope compensation and the duty cycle  $D$  can be expressed as [7]:

$$m > (1 - \frac{1}{2D})m_2 \tag{2}$$

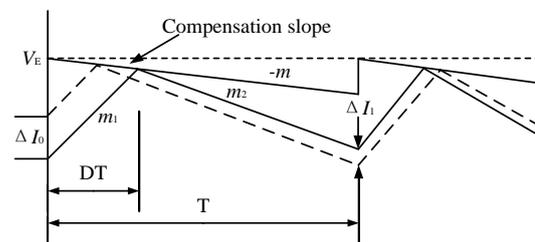


FIGURE 3 In the situation of  $D > 50\%$ , the stability of system is realized when slope compensation is introduced

This is the basic principle of slope compensation. And two conventional ways are the fixed slope compensation and the piecewise linear slope compensation. However, both of them may bring excessive compensation (or under compensation), resulting in lower transient response and load capability of switching power supply.

**3.2 THE BAISC METHOD OF DYNAMIC SLOPE COMPENSATION**

According to the drawbacks of fixed slope compensation and piecewise linear slope compensation, this paper presents a method of dynamic slope compensation. Specifically, for the Boost DC-DC converter shown in Figure 1, the rise and fall slope of inductive current can be expressed as [8]:

$$m_1 = \frac{V_{IN}}{L} R_{DSON}, \tag{3}$$

$$m_2 = \frac{V_{OUT} - V_{IN}}{L} R_{DSON}, \tag{4}$$

where  $L$  is the inductive value and  $R_{DSON}$  is the resistance of switch.

Using Equations (3) and (4), Equation (1) can be reversed as:

$$m > \frac{0.5V_{OUT} - V_{IN}}{L} R_{DSON}. \tag{5}$$

The system can remain stable as long as the input voltage  $V_{IN}$ , the output voltage  $V_{OUT}$  and the slope  $m$  of the slope compensation signal satisfy Equation (5). Therefore, we can achieve dynamic slope compensation by adjusting compensation slope following the variation of input and output voltage, so that excessive compensation can be eliminated and the load capacity of the system can be enhanced.

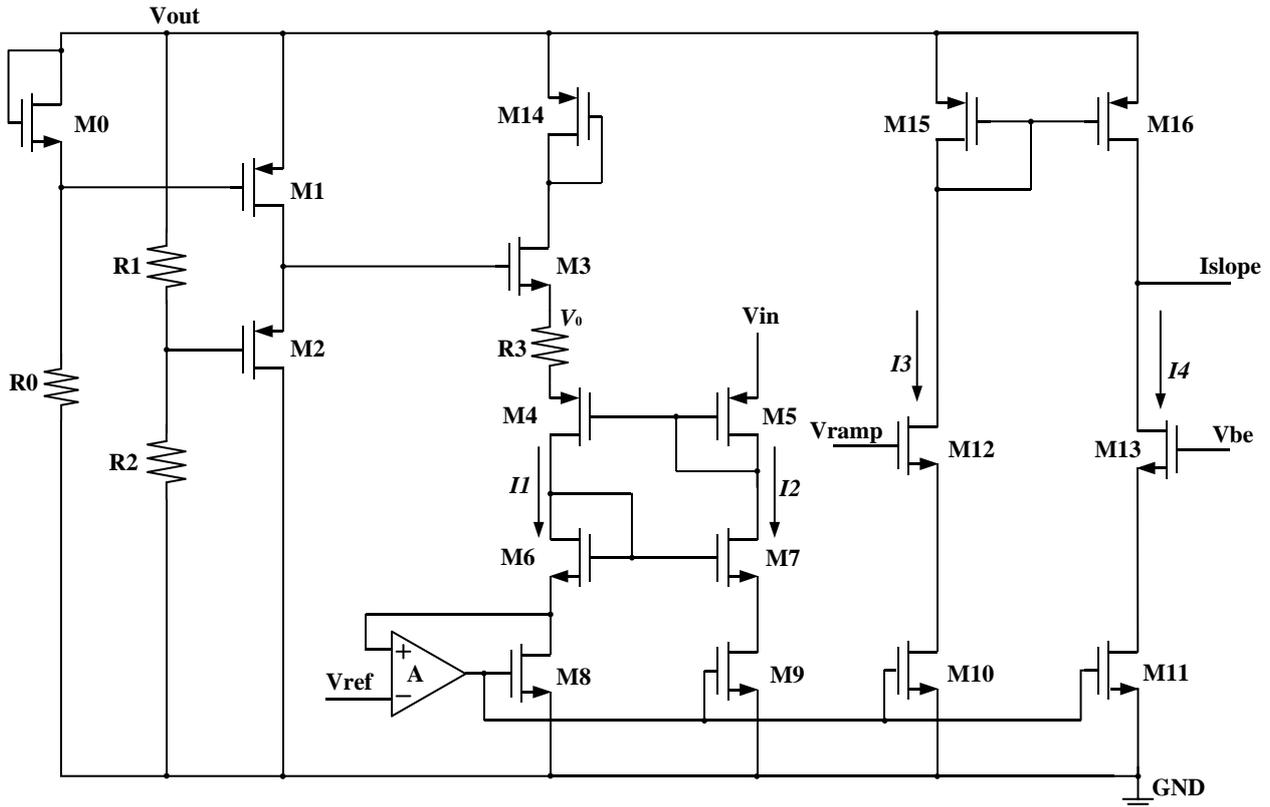


FIGURE 4 Dynamic slope compensation circuit

### 3.3 DYNAMIC SLOPE COMPENSATION CIRCUIT DESIGN

Figure 4 is the dynamic slope compensation circuit designed in this paper, where M0, M1, M2, M3, R0, R1, R2, R3 constitute a voltage divider network producing a regulated output voltage, and M4, M5, M6, M7 constitute cascode current mirror producing current  $I_1$  following the variation of input and output voltage. M8, M9, M10, M11 work in the linear region and can be equivalent to resistances whose values are controlled by the overdrive voltage. Operational amplifiers A working as a voltage follower adjust the equivalent resistance of M8. The slope compensation current  $I_{SLOPE}$  is outputted after the slope conversion of sawtooth signal  $V_{RAMP}$ . M14, M15, M16 constitute current mirror.

Specifically, M0 and R0, M1 and M2, M3 and R3 form a source follower, R1 and R2 form a voltage divider

network. By adjusting the W/L of M0, M1, M2, M3 and other related parameters to get  $|V_{GS2}|=V_{GS3}$ , we obtain:

$$V_0 = \frac{R_2}{R_1 + R_2} V_{OUT}. \tag{6}$$

To get the current following the variation of input and output voltage, we introduce cascode current mirror as clamp circuit and let the W/L of M4, M5 and M6, M7 equal respectively, which make  $I_1=I_2$  and source voltage of M4 equal to  $V_{IN}$ , therefore:

$$I_1 = \frac{(V_0 - V_{IN})}{R_0}. \tag{7}$$

With Equation (6), Equation (7) can be rewritten as:

$$I_1 = \frac{((R_2/(R_1 + R_2))V_{OUT} - V_{IN})}{R_0}. \tag{8}$$

The inverse of the operational amplifier A is provided by a 0.2V reference voltage, which makes the drain voltage of M8 equal to 0.2V, so that it can work in linear region. Then, the resistance of it can be expressed as:

$$R_{M8} = \frac{0.2}{I_1} = \frac{0.2R_0}{(R_2/(R_1 + R_2))V_{OUT} - V_{IN}} \quad (9)$$

The on-resistances of MOS tubes working in linear region can be expressed as [9]:

$$R_{DS} = \frac{1}{\mu C_{OX}(V_{gs} - V_{th})(W/L)} \quad (10)$$

When the gate voltage and source voltage of M8, M9, M10, M11 equal respectively, they have the same  $V_{gs}$ . As long as the W/L of these four tubes are equal, they can work in linear region and have the same on-resistance, which can be expressed as:

$$R_{M8} = R_{M9} = R_{M10} = R_{M11} = \frac{0.2R_0}{(R_2/(R_1 + R_2))V_{OUT} - V_{IN}} \quad (11)$$

In Figure 4, M10, M11, M12, M13 constitute slope conversion circuit with a source negative feedback, if  $R_{M10} \gg \frac{1}{g_{m12}}$ , drain current of M12 can be thought as a linear function of its own input gate voltage. We obtain:

$$I_3 \approx \frac{V_{RAMP} - V_{th}}{R_{M10}} \quad (12)$$

Similarly, if  $R_{M11} \gg \frac{1}{g_{m13}}$ , we obtain:

$$I_4 \approx \frac{V_{BE} - V_{th}}{R_{M11}} \quad (13)$$

Make the W/L of M15, M16 equal, as  $R_{M10} = R_{M11}$ , according to the current mirror relationship, we obtain:

$$I_{SLOPE} = I_3 - I_4 = \frac{V_{RAMP} - V_{BE}}{R_{M10}} \quad (14)$$

$$= \frac{(V_{RAMP} - V_{BE})((R_2/(R_1 + R_2))V_{OUT} - V_{IN})}{0.2R_0}$$

We can get the slope of compensation signal by (14):

$$m_{SLOPE} = \frac{(R_2/(R_1 + R_2))V_{OUT} - V_{IN}}{0.2R_0} m_{RAMP} \quad (15)$$

As a result, we can choose resistances of R0, R1, R2 according to the slope  $m_{RAMP}$  of sawtooth signal so that the following formula can be satisfied:

$$\frac{1}{0.2R_0} m_{RAMP} > \frac{1}{L} R_{DSON} \quad (16)$$

Thereby, we can adjust the slope of slope compensation circuit following the variation of input and output voltage to eliminate excessive compensation phenomenon and achieve the stability of the current loop.

#### 4 Simulation results and analysis

Based on peak current mode Boost DC-DC converter shown in the Figure 1, the dynamic slope compensation circuit is simulated on Cadence Spectre using SMIC 0.18μm CMOS technology. Figure 5a) is the changes of compensation slope when the input voltage is 1.8 V and the range of output voltage is 4 V to 7 V. Figure 5b) shows changes of the compensation slope when the output voltage is 4 V and the range of input voltage is 2.3 V to 3.3 V. As we can see, the compensation slope has been increased with the duty cycle changing from 55% to 75%, and the compensation slope decreases with the increasing of input voltage.

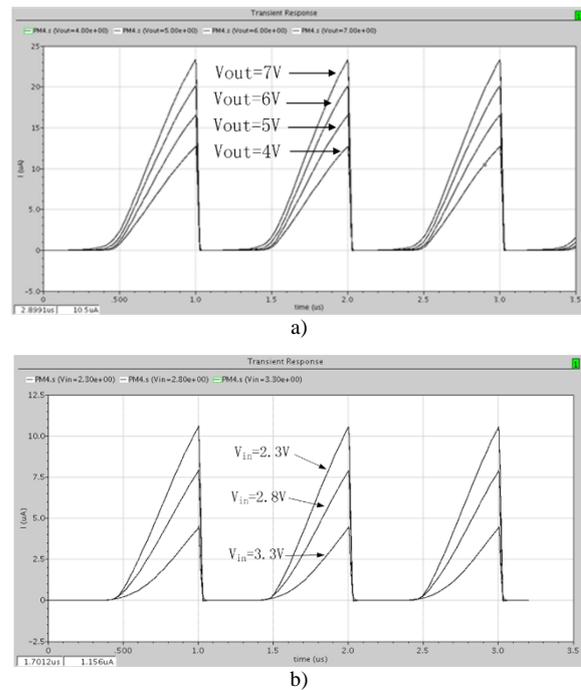


FIGURE 5 Slope compensation current with the changes in  $V_{IN}$  and  $V_{OUT}$ : a)  $V_{IN}=1.8V$ , b)  $V_{OUT}=4V$

The PWM waveforms shown in Figure 6 are simulated in peak current mode Boost DC-DC converter with the dynamic slope compensation circuit working in steady state. Where, the simulation parameters are  $V_{IN}=1.8V$ ,  $V_{OUT}=4V$ ,  $L=2.2\mu H$ ,  $C=10\mu F$ ,  $f=1MHz$ . As we can see, under the condition of duty cycle  $D=55\%$ , the inductive current is constant at 550mA and sub-harmonic oscillation phenomenon did not occur. Therefore, the compensation circuit designed in this paper works properly and the loop is stable.

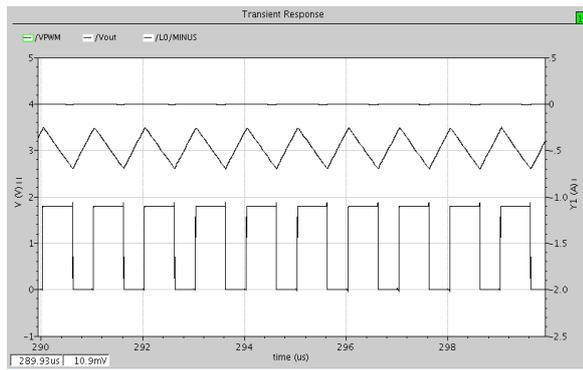


FIGURE 6 Simulation waveform under PWM

Figure 7 shows the transient response simulation waveform of DC-DC converter when rise and fall time are  $1\mu s$  and amplitude of square load current is  $200mA$  in  $V_{IN}=1.8V$ ,  $V_{OUT}=4V$ . The response time of the output voltage is less than  $10\mu s$ , voltage overshoot is only  $80 mV$ , and there is no ringing. The system works stable.

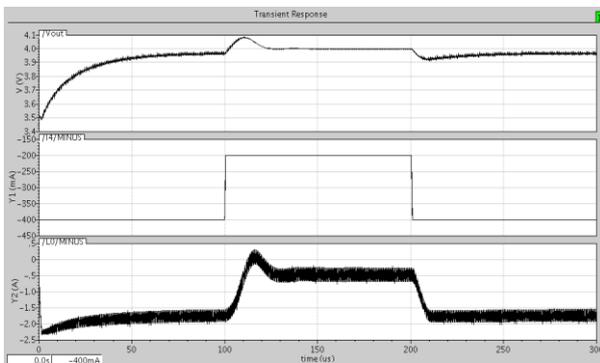
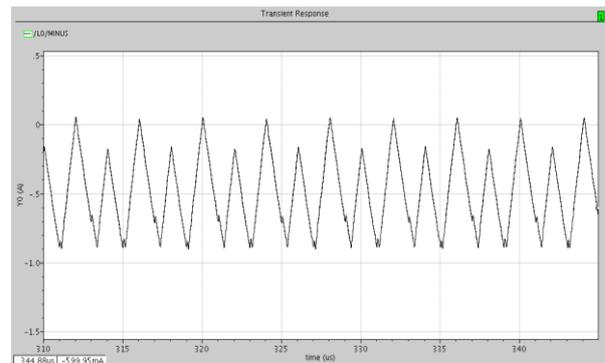


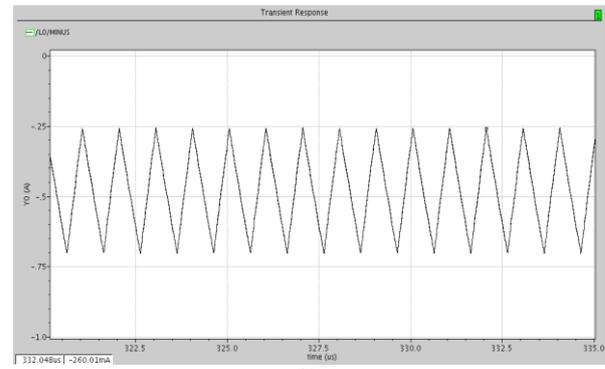
FIGURE 7 Load transient response waveform

Finally, in the case of load current is constant at  $550mA$ , we simulate the whole DC-DC converter with the slope compensation circuit and without the slope compensation circuit respectively to further verify the stability of the

system when the duty cycle is over 50%. The simulation result is shown in Figure 8. The oscillation of inductive current is serious and the inductive current is instable when slope compensation circuit is not introduced. On the contrary, when the slope compensation circuit is introduced, the inductive current is constant at  $550mA$ .



a)



b)

FIGURE 8 Inductor current simulation waveform: a) Without slope compensation, b) With slope compensation

The comparison of the main technical parameters of the circuit designed in this paper and other typical slope compensation circuits is shown in Table 1.

TABLE 1 Comparison between circuit in this paper and other typical slope compensation circuits

Parameter	This paper	Reference [9]	Reference [10]
technology ( $\mu m$ )	0.18	0.8	0.25
input voltage (V)	1.8-4	2.5-5	3.3-12
output voltage (V)	4	6	3.3
load current (mA)	550	500	800
voltage overshoot (mV)	80	100	150
transient response time ( $\mu s$ )	10	30	70

### 5 Conclusions

This paper proposed a new method of dynamic slope compensation and designed a dynamic slope compensation circuit with simple structure based on the traditional slope compensation. Simulation results show that this circuit can provide proper slope compensation signal for peak current Boost DC-DC converter, as well as faster transient response, slighter voltage overshoot and higher load

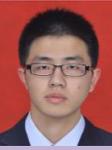
current. More importantly, the results show that the circuit can eliminate excessive compensation and open-loop instability, and realize stable operation of the system.

### Acknowledgments

This work is supported by Promotion of Development in Science and Technology Services Project in Guangdong Province, China (No.2011B040300035).

## References

- [1] Qun Z, Lee F C 2003 *IEEE Transactions on Power Electronics* **18**(1) 65-73
- [2] Lee C F, Mok P K T 2004 *IEEE Journal of solid-state circuits* **39**(1) 3-14
- [3] Liaw C M, Chiang S J, Lai C Y, Pan K H, Leu G C 1994 *IEEE Transactions on Industrial Electronics* **41**(2) 231-40
- [4] Hu S, Zou X, Zhang J Kong L 2007 A new dynamic slope compensation circuit applied to boost DC-DC converter *Computer and Digital Engineering* **35**(10) 159-62 (in Chinese)
- [5] Chen F, Lai X, Li Y 2008 Design and implementation of an adaptive slope compensation circuit *Journal of Semiconductors* **29**(3) 593-7 (in Chinese)
- [6] Canesin C A, Barbi I 1996 *IEEE Applied Power Electronics Conference and Exposition San Jose* **2** 807-13
- [7] Bryant B, Kazimierczuk M K 2005 *IEEE Transactions on Circuits and Systems* **52**(11) 2404-12
- [8] Lu J, Wu X 2007 *IEEE Electron Devices and Solid-State Conference* 929-32
- [9] Wang L, Wang S, Lai X, Tian J 2007 Design of a piecewise linear slope compensation circuit for peak current mode boost DC-DC converter *Research & Progress of SSE* **27**(2) 269-74 (in Chinese)
- [10] Guoding Dai, Yang Xu, Weimin Li and Bo Hu. 2012 The design and realization of internal compensation circuit for current mode PWM step-down DC-DC converters *Electron Devices* **33**(1) 53-7 (in Chinese)

Authors	
	<p><b>Zhao Han, born in February, 1990, Jincheng, Shanxi, P.R. China</b></p> <p><b>Current position, grades:</b> Master student at the School of Information Science and Technology, Jinan University, China.  <b>University studies:</b> B.Sc. at College of Information and Business at North University of China in China (2008-2012).  <b>Scientific interest:</b> power management units and analogue integrated circuits designs.  <b>Experience:</b> studying in the field of analogue integrated circuit design for 2 years, 1 scientific research project.</p>
	<p><b>Yuan Rao, born in May, 1989, Wuzhou, Guangxi, P.R. China</b></p> <p><b>Current position, grades:</b> Master student at the School of Information Science and Technology, Jinan University, China.  <b>University studies:</b> B.Sc. at the International School at Beijing University of Posts and Telecommunications in China (2007-2011).  <b>Scientific interest:</b> analogue integrated circuits designs, system on chip designs, power management units.  <b>Publications:</b> 3 papers.  <b>Experience:</b> studying in the field of analogue integrated circuit design for 3 years, 2 scientific research projects.</p>
	<p><b>Wentao Chen, born in February, 1990, Longyan, Fujian, P.R. China</b></p> <p><b>Current position, grades:</b> Master student at the School of Information Science and Technology, Jinan University, China.  <b>University studies:</b> B.Sc. at the school of microelectronics at Xidian University in China (2008-2012).  <b>Scientific interest:</b> analogue integrated circuits designs and system on chip designs.  <b>Publications:</b> 1 paper submitted.  <b>Experience:</b> studying in the field of analogue integrated circuit design for 2 years.</p>
	<p><b>Junkai Huang, born in October, 1963, Shantou, Guangdong, P.R. China</b></p> <p><b>Current position, grades:</b> Ph.D. degree, Professor at the School of Information Science and Technology, Jinan University, China. Director of the Department of Electronic Engineering and the Vice President of the School of Information Science and Technology in Jinan University.  <b>University studies:</b> B.Sc. and M.Sc. at the School of Information Science and Technology from Jinan University in China. Ph.D. at South China University of Technology in China.  <b>Scientific interest:</b> Thin-film material and devices, application specific integrated circuit chips.  <b>Publications:</b> more than 50 papers.  <b>Experience:</b> teaching experience of 30 years.</p>